

Claims

- [c1] An IC comprising:
- a memory cell array having a plurality of memory cells;
 - a first and a second port, each of said memory cells being coupled to said first and second ports;
 - a cache memory coupled to said first and second ports, wherein during a read operation subject to one of said memory cells through one of said first and second ports a data stored in said one of said memory cells is read out from said cache memory if it is determined that said cache memory contains said data stored in said one of said memory cells; and
 - a refresh control circuit performing a refresh of the information stored within said memory cells, said refresh control circuit refreshing memory cells through one of said ports while reading data out of said cache memory.
- [c2] The IC according to claim 1, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said corresponding address and data portions contain valid address and data values.
- [c3] The IC according to claim 2, wherein said first and second ports each comprises an address path and a data read path, said address paths of said first and second ports being connected to said address portion of said cache memory and said data read paths of said first and second ports being connected to said data portion.
- [c4] / The IC according to claim 3, wherein said cache memory comprises an address comparator which is coupled to said address path of at least one of said first and second ports.
- [c5] / The IC according to claim 4, wherein said address comparator is designed to compare an address being provided through said at least one of said ports and an address being provided from said address portion of said address memory, and in case of a match designed to output the data stored in the corresponding memory cell onto the read path of said at least one port.

- [c6] The IC according to claim 5, wherein in case of said match of addresses a refresh for a row of memory cells within the memory cell array is performed through the second port.
- [c7] The IC according to claim 6, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.
- [c8] The IC according to claim 7, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.
- [c9] ✓ The IC according to claim 5, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.
- [c10] ✓ The IC according to claim 9, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.
- [c11] ✓ The IC according to claim 1, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.
- [c12] ✓ The IC according to claim 11, wherein said storage node comprises a storage transistor, a drain-source-path of said storage transistor being coupled between said first and second selection transistors, and a control terminal of said storage transistor being coupled to a reference potential.
- [c13] An IC comprising:
a memory cell array having a plurality of dynamic

memory cells;
a first port and a second port for performing an access to at least one of said memory cells;
a refresh control circuit to perform a refresh for said memory cells once within a retention time interval;
a cache memory connected to at least one of said ports;
a switching device coupled to said at least one of said ports, said cache memory, and said memory cell array; and
said switching device being operated to connect either one of said memory cell array and said cache memory to said at least one of said ports in response to a read operation.

[c14] The IC according to claim 13, wherein said refresh control circuit performs a refresh operation while a read operation is performed through said at least one of said ports from said cache memory.

[c15] The IC according to claim 13, wherein said cache memory comprises a tag portion, an address portion, and a data portion corresponding to each other, wherein said tag portion indicates if said address and data portions contain valid address and data values.

[c16] The IC according to claim 13, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.

[c17] A IC comprising:
a memory cell array;
a first and a second port coupled to each one of said memory cells;
a cache memory coupled to said first and second ports;
said first and second ports comprising address terminals and data terminals;
and
said second port being controlled by a refresh control circuit to perform a refresh of said memory cells.

- [c18] The IC according to claim 17, wherein a refresh operation is performed for a row of memory cells through said second port, and a read command received through said second port is performed through said cache memory in parallel to said refresh operation.
- [c19] The IC according to claim 17, wherein each memory cell of said memory cell array comprises a first selection transistor coupled to said first port and a second selection transistor coupled to said second port and a storage node connected to said first and second selection transistors.